CLAIMS

Please amend the claims as follows.

1. (Currently amended) A data recovery apparatus for a digital data stream of input data, comprising:

phase shifting means for outputting a plurality of sampling clocks in a bit time, where the phase of ~~of~~ said plurality of sampling clocks are ~~automatically~~ adjustable ~~and where a time distance between a first-occurring clock of the plurality of clocks and a last-occurring clock of the plurality of clocks is automatically adjustable~~;

data sampling means for sampling the input data using the sampling clocks as triggers, and for providing multiple sampled data signals, where one of said sampled data signals is used to output recovered data;

compare logic means for comparing said sampled data signals to said recovered data and providing at least a first pseudo-bit error value and a second pseudo-bit error value; and

phase controlling means for estimating the phase relationship between the input data and said plurality of sampling clocks using ~~the comparison result of said compare logic means~~ at least said first pseudo-bit error value and said second pseudo-bit error value, and for providing control signals to said phase shifting means according to said estimation results.

2. (Previously presented) The apparatus of claim 1 wherein the phase shifting means comprises:

phase delay means controlled by a first output of said phase controlling means for outputting a first sampling clock of said plurality of sampling clocks

using an input clock which is one of an external clock and an internally recovered clock;

first circuit means controlled by a second output of said phase controlling means for outputting a second sampling clock of said plurality of sampling clocks that advances said first sampling clock in phase;

second circuit means controlled by the second output of said phase controlling means for outputting a third sampling clock of said plurality of sampling clocks that is delayed from said first sampling clock in phase; and

the phases of the three sampling clocks are arranged within an eye opening of the input data stream with a predetermined margin.

3. (Original) The apparatus of claim 2, wherein the first circuit means and the second circuit means receive the first sampling clock.

4. (Previously presented) The apparatus of claim 1, wherein the phase shifting means comprises:

a phase distributor outputting a plurality of phase shift values;

a buffer receiving input from the phase distributor and outputting a first sampling clock of the plurality of sampling clocks in accordance with a first output of said phase controlling means; and

selection logic receiving input from the phase distributor and outputting a second and third sampling clock of the plurality of sampling clocks in accordance with a second output of said phase controlling means.

5. (Original) The apparatus of claim 1 wherein the phase shifting means comprises:

a voltage controlled oscillator controlled by a first output of the phase controlling means, circuit means controlled by a second output of said phase controlling means for outputting three sampling clocks by delaying the output of the voltage controlled oscillator, where the phases of the three sampling clocks are arranged within an eye opening of input data stream with a predetermined margin.

6. (Currently amended) A data recovery apparatus for a digital data stream of input data, comprising:

a phase shifter that outputs a plurality of sampling clocks in a bit time, where the phase of said plurality of sampling clocks are ~~automatically~~ adjustable ~~and where a time distance between a first occurring clock of the plurality of clocks and a last occurring clock of the plurality of clocks is automatically adjustable~~;

a data sampler that samples the input data using the sampling clocks as triggers, and for providing multiple sampled data signals, where one of said sampled data signals is used to output recovered data;

compare logic that compares said sampled data signals to said recovered data and provides at least a first pseudo-bit error value and a second pseudo-bit error value; and

a phase controller that ~~estimating~~ estimates the phase relationship between the input data and said plurality of sampling clocks using ~~the comparison result of said compare logic means~~ at least said first pseudo-bit error

value and said second pseudo-bit error value, and for providing control signals to said phase ~~shifting means~~ shifter according to said estimation result.

7. (Previously presented) The apparatus of claim 6 wherein the phase shifter comprises:

phase delay logic controlled by a first output of said phase controller for outputting a first sampling clock of said plurality of sampling clocks using an input clock which is one of an external clock and an internally recovered clock;

a first circuit, controlled by a second output of said phase controller, for outputting a second sampling clock that advances said first sampling clock of said plurality of sampling clocks in phase;

a second circuit, controlled by the second output of said phase controller, for outputting a third sampling clock of said plurality of sampling clocks that is delayed from said first sampling clock in phase; and

the phases of the three sampling clocks are arranged within an eye opening of the input data stream with a predetermined margin.

8. (Currently Amended) The apparatus of claim 6 wherein the phase shifter comprises:

a voltage controlled oscillator controlled by a first output of the phase controller, a circuit, controlled by a second output of said phase ~~control~~ controller, for outputting three sampling clocks by delaying the output of the voltage controlled oscillator, where the phases of the three sampling clocks are arranged within an eye opening of input data stream with a predetermined margin.

9. (Currently Amended) A data recovery method for a digital data stream, comprising:

sampling input data at multiple points, where said sampling points are arranged by a predetermined order and adjustable time difference;

providing a first pseudo bit-error signal from a comparer that is a result of comparison of data sampled at an early boundary with recovered data;

providing a second pseudo bit-error signal from said comparer that is a result of comparison of data sampled at a late boundary with recovered data; and

using the first and second pseudo bit-error signals, so that the sampling boundary is marginally matched to the edge of an eye opening and one of the intermediate sampling points serves for data recovery.

10. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 1, wherein the phase of said plurality of sampling clocks are automatically adjustable.

11. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 10, wherein a time distance between a first-occurring clock of the plurality of clocks and a last-occurring clock of the plurality of clocks is automatically adjustable.

12. (New) A data recovery apparatus for a digital data stream of input data, as recited in Claim 6, wherein said phase of said plurality of sampling clocks are automatically adjustable.

13. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 12, wherein a time distance between a first-occurring clock of the plurality of clocks and a last-occurring clock of the plurality of clocks is automatically adjustable.

14. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 6, wherein said data sampler comprises:

a first latch operably coupled to receive a first clock signal, said first latch capable of providing a first sample of data,

a second latch operably coupled to receive a second clock signal, said second latch capable of providing a second sample of data, and

a third latch operably coupled to receive a second clock signal, said third latch capable of providing a third sample of data.

15. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 14, wherein said compare logic comprises:

a first XOR gate operably coupled to receive said first sample of data and said second sample of data, said first XOR gate capable of providing a first comparison output, and

a second XOR gate operably coupled to receive said third sample of data and said second sample of data, said second XOR gate capable of providing a second comparison output.

16. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 15, wherein said compare logic further comprises:

a first latch operably coupled to receive said first comparison output, said first latch capable of providing a first latched output, and

a second latch operably coupled to receive said second comparison output, said second latch capable of providing a second latched output.

17. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 16, wherein said phase controller comprises:

a first phase estimator operably coupled to receive said first latched output and said second latched output, said first phase estimator capable of providing a first phase estimate output, and

a second phase estimator operably coupled to receive said first latched output and said second latched output, said second phase estimator capable of providing a second phase estimate output.

18. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 17, wherein said phase controller further comprises:

a first loop filter operably coupled to receive said first phase estimate output, said first loop filter capable of providing a first filtered output, and

a second loop filter operably coupled to receive said second phase estimate output, said second loop filter capable of providing a second filtered output.

19. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 18, wherein said phase shifter is operably coupled to receive said first filtered output and said second filtered output, said phase shifter capable of providing said first clock signal, said second clock signal, and said third clock signal.

20. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 17, wherein said first phase estimate output is the difference between said first latched output and said second latched output.

21. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 20, wherein said second phase estimate output is the sum of said first latched output and said second latched output.

22. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 17, wherein said first phase estimate output is the weighted difference between said first latched output and said second latched output.

23. (New) A data recovery apparatus for a digital data stream of input data as recited in Claim 20, wherein said second phase estimate output is the weighted sum of said first latched output and said second latched output.